LATERAL THIN-FILM SOI DEVICE HAVING A FIELD PLATE WITH ISOLATED METALLIC REGIONS

The present invention relates to thin-film Semiconductor-On-Insulator (SOI) devices, and more particularly to a field plate with laterally isolated metallic regions used in such devices, which forms a linear lateral electric field to eliminate an electric field enhancement.

A field plate is used in a Semiconductor-On-Insulator (SOI) device to shield the drift region of the device from package and surface charge effects, which may be caused by moisture or other charged containments on the surface of the wafer. The field plate is usually of metallic material, and is connected to, or an extension of, the source region or the gate electrode, such as in US Patent Nos. 6,127,703 and 5,412,241, commonly-assigned with the instant application and incorporated herein by reference.

However, such a field plate may bring an electric field enhancement at the edge of the field plate, which results in electron injection into the interlevel dielectric. This problem is more profound in a high voltage SOI PMOS device where the drift region has a linearly-graded charge profile. The device may break down well before the specified voltage due to the high electric field at the end of the field plate. In practice, the device exhibits charge injection into the dielectric layer in the region of high electric field to reduce the imposed field.

US patent No. 6,246,101 issued to Akiyama describes an isolation field plate chain structure for a high voltage device in which voltage is supported vertically in the device by depletion of the pn junction of plate chain formed by the field plate chain. Thus, the lateral electric field is specified by design of the capacitive field plate

chain, which is thus complicated in component design. The doping in the drift region does not determine the lateral electric field.

Thus, there is a need for a field plate with simple structure and design, in which the electric field enhancement is eliminated.

To realize the above goal, the present invention provides a lateral thin-film Silicon-On-Insulator (SOI) device which comprises a semiconductor substrate, a buried insulating layer on the substrate, and a lateral MOS transistor device in an SOI layer on the buried insulating layer and having a source region of a first type of conductivity formed in a body region of a second type conductivity, a lateral drift region of a second type conductivity adjacent the body region, a drain region of a first conductivity and laterally spaced apart from the body region by the lateral drift region, a gate electrode insulated from the body region and drift region by an insulation region, and a field plate extending substantially over the lateral drift region. In particular, according to the present invention, the field plate comprises a layer of plural metallic regions which are isolated laterally from one another by spacing so as to form a linear lateral electric field distribution. Preferably the field plate is an extension of the source region. Thus, the voltage in the isolated regions is linearly distributed laterally, and drops lineally to a lower value at the end of the field plate. This prevents a sudden large voltage change across the geometry of the device, and the large electric field that would otherwise result.

Preferably, the transistor is a PMOS transistor in which the lateral drift region has a linearly-graded charge profile, and the voltage drop in the field plate follows the electric field in the drift region.

Preferably, the device comprises another metallic region located above the spacing in the first layer, and isolated from the first layer as well.

The isolated metallic regions are preferably embedded in a dielectric layer of high resististivity.

Further features and advantages of the present invention will become clearer after reading the detailed description of the preferred embodiment according to the present invention with a reference to the accompanying drawings, in which:

Figure 1 shows a simplified cross-sectional view of a first embodiment of a lateral thin-film SOI device according to the present invention; and

Figure 2 is similar to Figure 1, but shows a second embodiment of a lateral thin-film SOI device according to the present invention.

As shown in Figure 1, a lateral thin-film device, here an SOI PMOS transistor 20, comprises a semiconductor substrate 22, a buried insulating layer 24, and a semiconductor surface SOI layer 26 in which the device is fabricated. The PMOS transistor includes a source region 28 of p-type conductivity, a body region 30 of n-type conductivity, a lateral drift region 32 of n-type conductivity, and a drain region 34 of p-type conductivity. The device also includes a gate electrode 36 which is completely insulated from the underlying semiconductor surface layer 26 and other conductive portions of the device by an oxide insulation region 38. Additionally, the transistor 20 further includes a body contact surface region 40, a surface-joining p-type conductivity drain extension region 46, a source contact electrode 42 which is tied to a high voltage +Vs, and a drain contact electrode 44.

A field plate is provided to extend laterally and substantially covers the lateral drift region 32. According to the present invention, the field plate comprises a segment or region 52a that is connected to, or an extension of, the source region 42.

The field plate also comprises a plural of isolated metallic segments or regions 52b, which are laterally isolated from one another, as well as from the region 52a, by spacing. Thus, only region 52a is tied to the high voltage +Vs of the source region 32. The field plate, which comprises the regions 52a and 52b, is embedded in a dielectric layer 53. The dielectric layer 53 is preferably a layer of high resistive silicon-rich silicon nitride.

Because of the isolation, unlike in the prior art where the voltage throughout the whole field plate is the same as the high voltage +Vs of the source region, the voltage in the field plate of the present invention is linearly distributed laterally. In other words, it drops linearly from the same high voltage +Vs of the source region 42 at its most left region (i.e., the region 52a) to a much lower value at the end of the field plate 52, i.e., at its most right region. Therefore, the electric field enhancement that existed in the prior art at the end of the field plate is eliminated.

Preferably, as shown in Figure 1, there is another layer of metallic regions 54 which are also embedded in the dielectric layer 53. Like metallic regions 52a, 52b, metallic regions 54 are laterally isolated from one another and from the metallic regions 52a, 52b as well, by means of the dielectric layer 53. The metallic regions 54 are located exactly above the isolation spacing or openings formed in the metallic regions 52a, 52b, so as to shield the spacing or openings in the metallic regions 52a, 52b from the package charge effects.

The lateral drift region 32 is preferably provided with a linearly-graded charge profile over at least a major portion of its lateral extent such that the doping level in the lateral drift region 32 increases in a direction from the drain region 34 toward the source region 28. In such a situation, the field plate preferably has a lateral electric

field distribution or profile that exactly follows the electric field in the SOI drift region 32.

Figure 2 shows another embodiment of the SOI device according to the present invention. Since the structure of this embodiment is similar to that in Figure 1, and like elements are referenced by like numerals for easy identification, only the differences are described here. In the embodiment shown in Figure 2, unlike in Figure 1 where the field plate comprises two layers of metallic regions 52a, 52b and 54, the field plate only comprises a layer of metallic regions. In particular, the filed plate in Figure 2 comprises a region 52a that is connected to, or an extension of, the source region 42, as well as isolated regions 52b. Because the isolation spacing in the metallic regions is not covered, thus the protection of package charge is less effective than that of the embodiment in Figure 1. It may be noted in this embodiment the isolating dielectric layer 53 does not cover the isolated metallic regions 52, and the metallic regions 52 are provided on another dielectric layer 50 between the field plate and the SOI layer 26.

The individual metallic regions can be patterned into any shape, and preferably have a size about 2x the smallest feature for the process. Alternatively, the relative width and spacing of the metallic regions can be defined so as to obtain a desired electric field profile.

Though the above has described in detail the preferred embodiments according to the present invention, it shall be appreciated that numerous changes, modifications and adaptations are possible to the those skilled in the art without departing the spirit of the present invention. For example, the SOI device may be a NMOS device instead of PMOS device, and the field plate 32 may be an extension, or connected to, the gate

electrode 36 instead of the source region 42, Thus, the scope of the invention is intent to be solely defined in the accompanying claims.